4-bit bus switch Rev. 7 — 11 April 2024

1. General description

The 74CBTLV3126 provides a 4-bit high-speed bus switch with separate output enable inputs (1OE to 4OE). The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The switch is disabled (high-impedance OFF-state) when the output enable (nOE) input is LOW.

To ensure the high-impedance OFF-state during power-up or power-down, nOE should be tied to the GND through a pull-down resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 2.3 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 2.3 V to 3.6 V
- Standard '126'-type pinout
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
 - 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

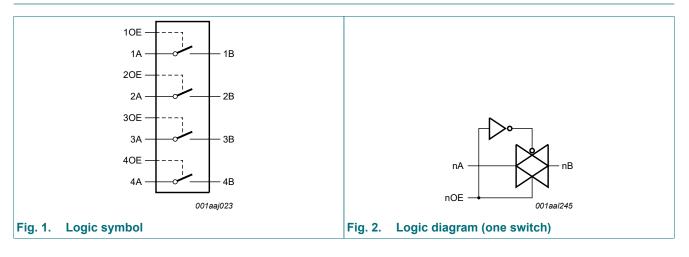
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3. Ordering information

Type number	Package								
	Temperature range	Name	Description	Version					
74CBTLV3126DS	-40 °C to +125 °C	SSOP16 [1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1					
74CBTLV3126PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1					
74CBTLV3126BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	<u>SOT762-1</u>					

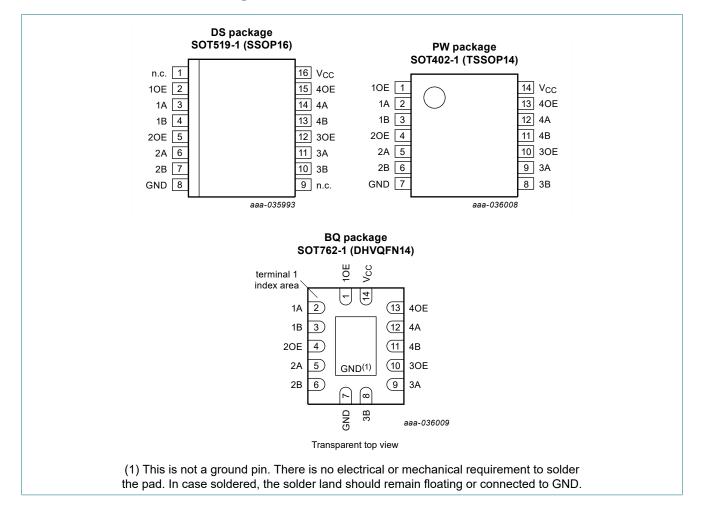
[1] Also known as QSOP16.

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Pin			
	SOT519-1	SOT402-1 and SOT762-1			
10E, 20E, 30E, 40E	2, 5, 12, 15	1, 4, 10, 13	output enable input		
1A, 2A, 3A, 4A	3, 6, 11, 14	2, 5, 9, 12	A input/output		
1B, 2B, 3B, 4B	4, 7, 10, 13	3, 6, 8, 11	B output/input		
GND	8	7	ground (0 V)		
V _{CC}	16	14	supply voltage		
n.c.	1, 9	-	not connected		

6. Functional description

Table 3. Function table

H = *HIGH* voltage level; *L* = *LOW* voltage level.

Output enable input nOE	Function switch
L	OFF-state
Н	ON-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
VI	input voltage	control inputs [1]	-0.5	+4.6	V
V _{SW}	switch voltage	enable and disable mode [2]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < -0.5 V	-50	-	mA
I _{SK}	switch clamping current	V _I < -0.5 V	-50	-	mA
I _{SW}	switch current	$V_{SW} = 0 V \text{ to } V_{CC}$	-	±128	mA
I _{CC}	supply current		-	+100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [3]	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input clamping current ratings are observed.

[2] The switch voltage ratings may be exceeded if switch clamping current ratings are observed

[3] For SOT519-1 (SSOP16) packages: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: Ptot derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		2.3	3.6	V
VI	input voltage	control inputs	0	3.6	V
V _{SW}	switch voltage	enable and disable mode	0	V _{CC}	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	pin nOE; V_{CC} = 2.3 V to 3.6 V	0	200	ns/V

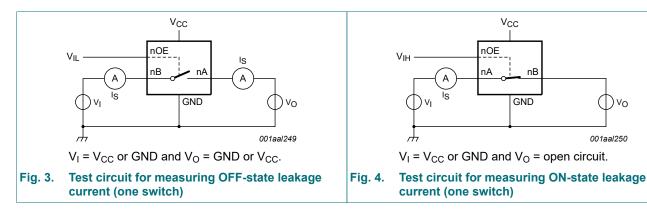
9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} :	= -40 °C to	+85 °C		_{nb} = o +125 °C	Unit
			Min	Typ [1]	Мах	Min	Max	-
VIH	HIGH-level input	V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
	voltage	V _{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
VIL	LOW-level input	V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
	voltage	V _{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
lı	input leakage current	pin nOE; V_1 = GND to V_{CC} ; V_{CC} = 3.6 V	-	-	±1.0	-	±20	μA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 3.6 V; see <u>Fig. 3</u>	-	-	±1	-	±20	μA
I _{S(ON)}	ON-state leakage current	V _{CC} = 3.6 V; see <u>Fig. 4</u>	-	-	±1	-	±20	μA
I _{OFF}	power-off leakage current	V ₁ or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±10	-	±50	μA
I _{CC}	supply current		-	-	10	-	50	μA
ΔI _{CC}	additional supply current	pin nOE; $V_1 = V_{CC} - 0.6 V;$ [2] $V_{SW} = GND \text{ or } V_{CC};$ $V_{CC} = 3.6 V$	-	-	300	-	2000	μA
CI	input capacitance	pin nOE; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	0.9	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance	V_{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	5.2	-	-	-	pF
C _{S(ON)}	ON-state capacitance	V_{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	14.3	-	-	-	pF

9.1. Test circuits



9.2. ON resistance

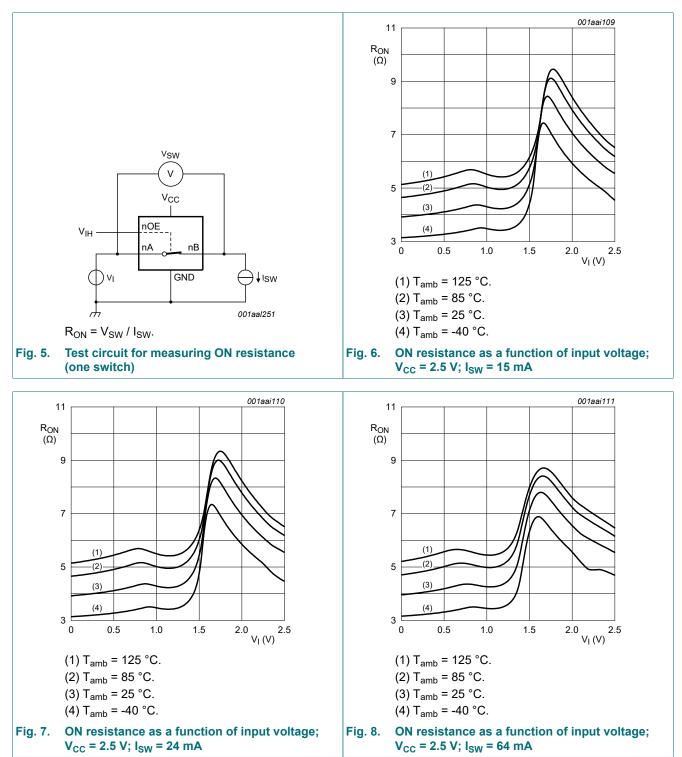
Table 7. Resistance RON

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol Parameter		Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Мах	Min	Max	
R _{ON}	ON resistance	V _{CC} = 2.3 V to 2.7 V; [2] see <u>Fig. 6</u> to <u>Fig. 8</u>						
		I _{SW} = 64 mA; V _I = 0 V	-	4.2	8.0	-	15.0	Ω
		I _{SW} = 24 mA; V _I = 0 V	-	4.2	8.0	-	15.0	Ω
		I _{SW} = 15 mA; V _I = 1.7 V	-	8.4	40.0	-	60.0	Ω
		V _{CC} = 3.0 V to 3.6 V; see <u>Fig. 9</u> to <u>Fig. 11</u>						
		I _{SW} = 64 mA; V _I = 0 V	-	4.0	7.0	-	11.0	Ω
		I _{SW} = 24 mA; V _I = 0 V	-	4.0	7.0	-	11.0	Ω
		I _{SW} = 15 mA; V _I = 2.4 V	-	6.2	15.0	-	25.5	Ω

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

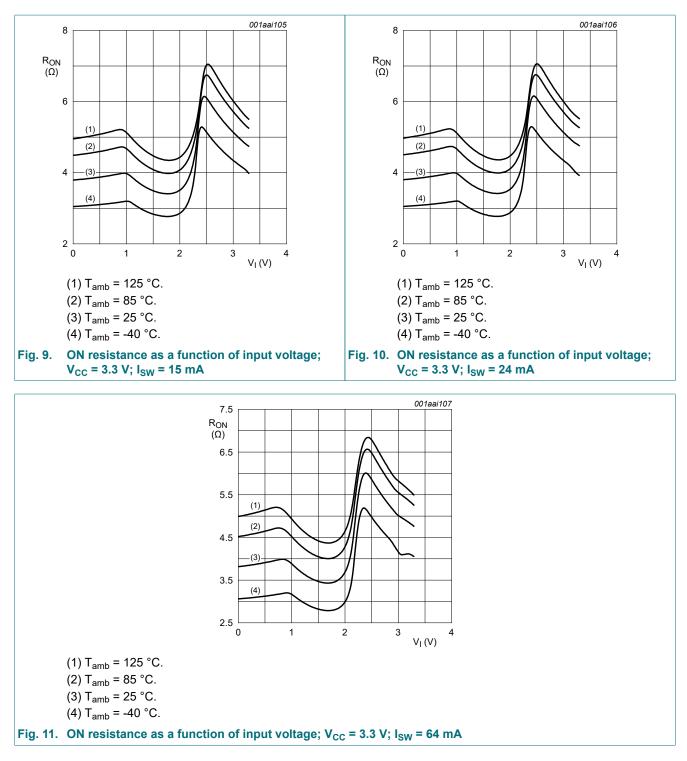
[2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



9.3. ON resistance test circuit and graphs

74CBTLV3126

4-bit bus switch



74CBTLV3126

10. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; for test circuit see Fig. 15

Symbol Parameter		eter Conditions		T _{amb} = -40 °C to +85 °C			T _{ar} -40 °C to	Unit	
				Min	Typ [1]	Мах	Min	Мах	
t _{pd}	propagation delay	nA to nB or nB to nA; see <u>Fig. 13</u>	[2] [3]						
		V _{CC} = 2.3 V to 2.7 V		-	-	0.13	-	0.20	ns
		V _{CC} = 3.0 V to 3.6 V		-	-	0.20	-	0.31	ns
t _{en}	enable time	nOE to nA or nB; see Fig. 14	[4]						
		V _{CC} = 2.3 V to 2.7 V		1.0	2.5	4.5	1.0	6.0	ns
		V _{CC} = 3.0 V to 3.6 V		1.0	2.2	4.2	1.0	6.0	ns
t _{dis}	disable time	nOE to nA or nB; see Fig. 14	[5]						
		V _{CC} = 2.3 V to 2.7 V		1.0	2.6	4.7	1.0	6.5	ns
		V _{CC} = 3.0 V to 3.6 V		1.0	3.4	4.8	1.0	6.5	ns

[1]

All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC} . The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, [2] when driven by an ideal voltage source (zero output impedance).

 t_{pd} is the same as t_{PLH} and t_{PHL} . [3]

[4] t_{en} is the same as t_{PZH} and t_{PZL} .

 t_{dis} is the same as t_{PHZ} and t_{PLZ} . [5]

10.1. Additional dynamic characteristics

Table 9. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);

Symbol	Parameter	Conditions			Unit	
			Min	Тур	Мах	
f _(-3dB)	-3 dB frequency response	$ V_I = GND \text{ or } V_{CC}; t_r = t_f \le 2.5 \text{ ns}; \\ V_{CC} = 3.3 \text{ V}; \text{ R}_L = 50 \Omega; \text{ see } \underline{\text{Fig. 12}} $	-	406	-	MHz

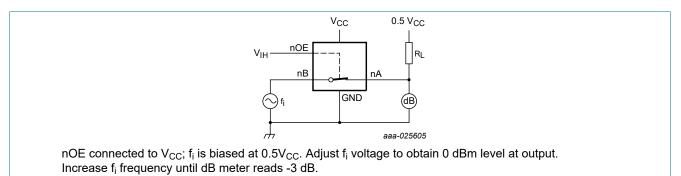


Fig. 12. Test circuit for measuring the frequency response when channel is in ON-state

10.2. Waveforms and test circuit

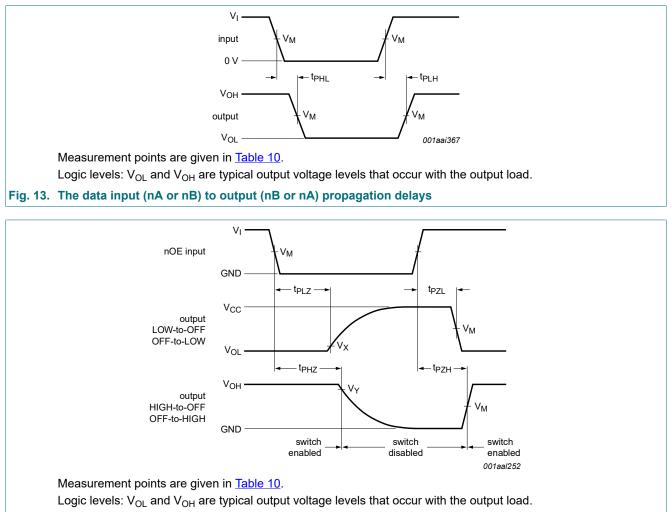


Fig. 14. Enable and disable times

Table 10. Measureme	nt points						
Supply voltage	Supply voltage Input			Output			
V _{cc}	V _M	Vi	V _M	V _X	V _Y		
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V _{CC}	$0.5 \times V_{CC}$	V _{OL} + 0.15 V	V _{OH} - 0.15 V		
3.0 V to 3.6 V	$0.5 \times V_{CC}$	V _{CC}	$0.5 \times V_{CC}$	V _{OL} + 0.3 V	V _{OH} - 0.3 V		

4-bit bus switch

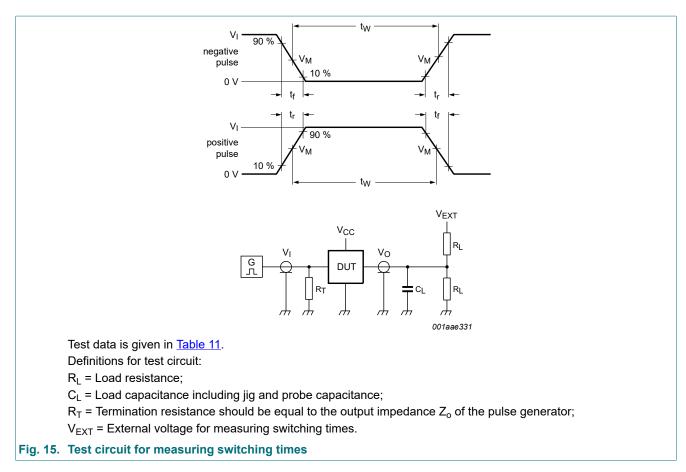


Table 11. Test data

Supply voltage	Load			V _{EXT}		
V _{cc}	CL	RL	t _r = t _f	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
2.3 V to 2.7 V	30 pF	500 Ω	≤ 2.0 ns	open	GND	2 × V _{CC}
3.0 V to 3.6 V	50 pF	500 Ω	≤ 2.0 ns	open	GND	2 × V _{CC}

11. Package outline

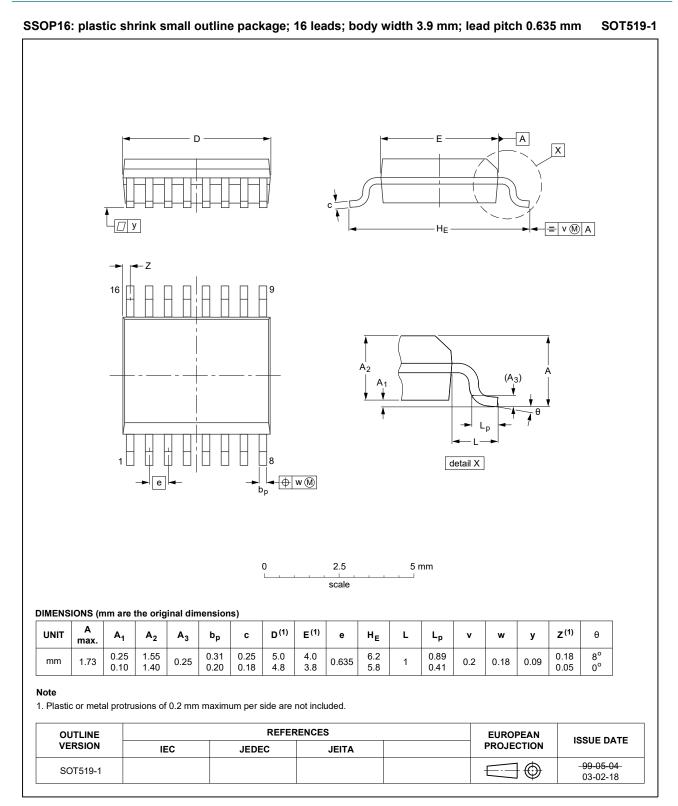


Fig. 16. Package outline SOT519-1 (SSOP16)

74CBTLV3126

4-bit bus switch

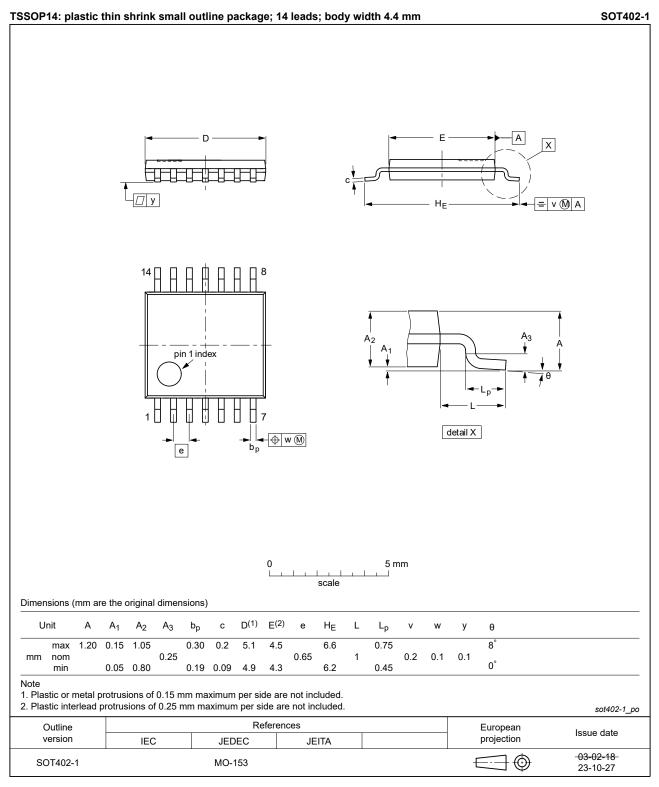


Fig. 17. Package outline SOT402-1 (TSSOP14)

4-bit bus switch

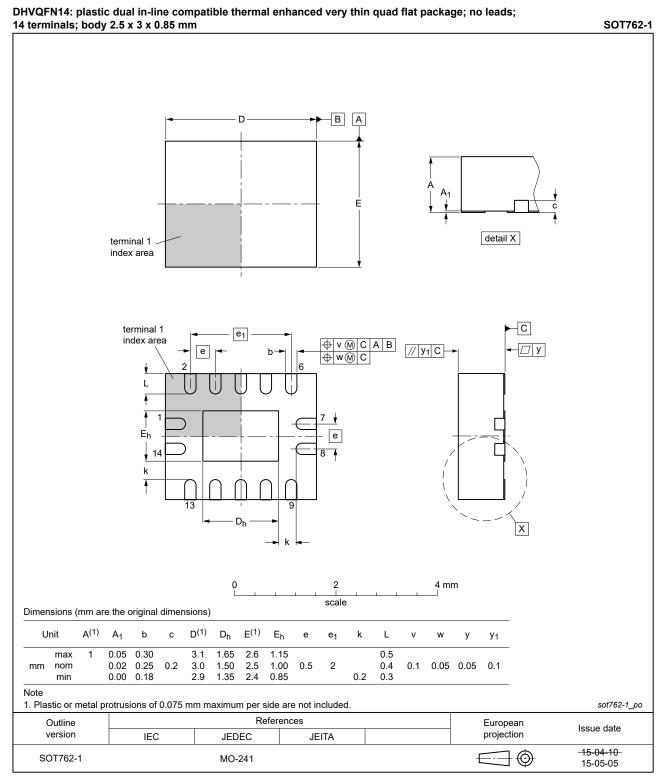


Fig. 18. Package outline SOT762-1 (DHVQFN14)

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12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74CBTLV3126 v.7	20240411	Product data sheet	-	74CBTLV3126 v.6		
Modifications:	• •	 Fig. 17: Aligned TSSOP package outline drawing to JEDEC MO-153. Section 2: ESD specification updated according to the latest JEDEC standard. 				
74CBTLV3126 v.6	20230216	Product data sheet	-	74CBTLV3126 v.5		
Modifications:	• <u>Section 7</u> : D	<u>Section 7</u> : Derating values for P _{tot} total power dissipation updated.				
74CBTLV3126 v.5	20181009	Product data sheet	-	74CBTLV3126 v.4		
Modifications:	of Nexperia	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 				
74CBTLV3126 v.4	20161108	Product data sheet	-	74CBTLV3126 v.3		
Modifications:	<u>Section 10.1</u> added.					
74CBTLV3126 v.3	20111215	Product data sheet	-	74CBTLV3126 v.2		
Modifications:	Legal pages updated.					
74CBTLV3126 v.2	20110104	Product data sheet	-	74CBTLV3126 v.1		
74CBTLV3126 v.1	20100105	Product data sheet	-	-		

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
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